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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,289	12/04/2003	Robert Francis Lembach	ROC920030229US1	7019

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EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,289	LEMBACH ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-20* is/are rejected.

7)☒ Claim(s) *1-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' Amendment to 10/728,289 has been examined. Claims 1, 3, 7, 11 and 17-20 are amended. Claims 1-20 are pending.

Applicants' Amendment is considered persuasive in part and the applicable rejections from the prior office action along with new ground of rejection are incorporated herein.

Claim Objections

2. Claims 1-20 are objected to because of the following informalities: The preamble must state the intended use or purpose of the invention. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the **second** paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. **Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Cannot determine the scope of applicant's invention based on independent claim 1 and its dependent claims.

5. **Claims 1-10 and 15 are rejected under 35 U.S.C. 112, second paragraph**, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: general lack of functional/structural relation among the claimed step in each claim. For example, in

claim 1, where is the origin of the inverting and non-inverting signal. In claim 3, the origin and destination of the inverting and non-inverting signal are unclear.

Regarding claim 7, it is unclear how the inverting and non-inverting signals relate to the rest of the claim.

Regarding claim 15, the specification does not clarify how the source and sink are in a chip without floorplans.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 11-16 are rejected under 35 U.S.C. 102(b)** as being anticipated by Sano et al. (U.S. Patent Application Publication No. US 2004/0107408).

As per **claim 11**, Sano discloses a signal-bearing medium encoded with instructions, wherein the instructions when executed comprise:

moving an inverting buffer from a source to a sink in a netlist ([0038]; [0080]; [0084]; [0086]; [0088]) if the source is to send both inverting and non-inverting signals from the source to the sink, wherein the moving further comprises

finding the inverting buffer associated with the source in the netlist ([0078]);

removing the inverting buffer associated with the source (Fig. 1, #546; [0174]);

adding the inverting buffer to the sink, wherein the sink is connected to the source via a plurality of routes (Fig. 1, #544; [0173]); and

removing at least one of the plurality of routes ([0092]).

As per **claim 12**, Sano discloses the signal-bearing medium of claim 11, wherein the adding is performed prior to chip placement, timing optimizations, and routing (Fig. 53; Fig. 54; [0027]; [0029]).

As per **claim 13**, Sano discloses the signal-bearing medium of claim 11, wherein the adding is performed after chip placement and before timing optimizations and routing (Fig. 21; Fig. 22; Fig. 23; Fig. 24; [0253]; [0254]; [0256]; [0273]; [0274]).

As per **claim 14**, Sano discloses the signal-bearing medium of claim 11, wherein the source represents a source region in a floorplanned chip and the sink represents a sink region in the floorplanned chip (Fig. 52, #285, #286, #287, #288; [0027]).

As per **claim 15**, Sano discloses the signal-bearing medium of claim 11, wherein the source and sink are in a chip without floorplans (Fig. 32; [0275]).

As per **claim 16**, Sano discloses the signal-bearing medium of claim 11, wherein the source and sink are in a same subpartition of a chip (Fig. 42; Fig. 43; [0295]; [0296]).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 7-10 and 17-20 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Sano in view of Dupenloup (US Patent No. 6,205,572). Sano discloses a clock tree circuit (Sano: Fig. 20B; [0250]) using buffer elements of two or more stages sending non-inverting signals from the source to the sink. However, Sano does not disclose a clock tree circuit using buffer elements that sends inverting signals from the source to the sink. Dupenloup also discloses a clock tree circuit (Dupenloup: Fig. 44; col. 74, line 25-35) using buffer elements of two or more stages sending non-inverting signals and includes inverting signals from the source to the sink that Sano does not disclose. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the inverting signal route of Dupenloup in the clock tree circuit of Sano since the circuit of Sano is not limited to only non-inverting signals from source to sink.

As per **claim 7**, Sano in view of Dupenloup discloses an apparatus comprising:

means for moving an inverting buffer from a source to a sink in a netlist (Sano: [0038]; [0080]; [0084]; [0086]; [0088]) if the source is to send both inverting and non-inverting signals from the source to the sink, wherein the means for moving further comprises

means for finding the inverting buffer associated with the source in a netlist (Sano: [0078]);

means for removing the inverting buffer associated with the source (Sano: Fig. 1, #546; [0051]; [0062]; [0174]); and

means for adding the inverting buffer to the sink, wherein the sink is connected to the source via a plurality of routes (Sano: Fig. 1, #544; Fig. 20A; [0051]; [0062]; [0173]), and wherein at least a first route of the plurality of routes is to send the inverting signals from the source to the sink and at least a second route of the plurality of routes is to send the non-inverting signals from the source to the sink (Dupenloup: Fig. 44; col. 74, line 25-35).

As per **claim 8**, Sano in view of Dupenloup discloses the apparatus of claim 7, further comprising:

means for removing the first route (Sano: [0092]).

As per **claim 9**, Sano in view of Dupenloup discloses the apparatus of claim 7, wherein the means for adding is performed prior to chip placement, timing optimizations, and routing (Sano: Fig. 53; Fig. 54; [0027]; [0029]).

As per **claim 10**, Sano in view of Dupenloup discloses the apparatus of claim 7, wherein the means for adding is performed after chip placement and before timing optimizations and routing (Sano: Fig. 21; Fig. 22; Fig. 23; Fig. 24; [0253]; [0254]; [0256]; [0273]; [0274]).

As per **claim 17**, Sano in view of Dupenloup discloses an electronic device comprising:

a processor (Sano: Fig. 1, #540; [0160]; and

a storage device encoded with instructions, wherein the instructions when executed on the processor comprise (Sano: [0164]; [0165]):

moving an inverting buffer from a source to a sink in a netlist (Sano: [0038]; [0080]; [0084]; [0086]; [0088]) if the source is to send both inverting and non-inverting signals from the source to the sink, wherein the moving further comprises

finding the inverting buffer associated with the source in the netlist (Sano: [0078]);

removing the inverting buffer associated with the source (Sano: [Fig. 1, #546; [0066]; [0174]);

adding the inverting buffer to the sink, wherein the sink is connected to the source via a plurality of routes, and wherein at least a first route of the plurality of routes is to send inverting signals and at least a second route of the plurality of routes is to send non-inverting signals (Dupenloup: Fig. 44; col. 74, line 25-35), and removing the first route (Sano: [0092]).

As per **claim 18**, Sano in view of Dupenloup discloses the electronic device of claim 17, wherein the source represents a source region in a floorplanned chip and the sink represents a sink region in the floorplanned chip (Sano: Fig. 52, #285, #286, #287, #288; [0027]).

As per **claim 19**, Sano in view of Dupenloup discloses the electronic device of claim 17, wherein the source and sink are in a chip without floorplans (Sano: Fig. 32; [0275]).

As per **claim 20**, Sano in view of Dupenloup discloses the electronic device of claim 17, wherein the source and sink are in a same subpartition of a chip (Sano: Fig. 42; Fig. 43; [0295]; [0296]).

Allowable Subject Matter

10. Claims 1-6 may be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: In a method of positioning inverting buffers in a netlist, the prior art does not teach moving an inverting buffer from a source to a sink in a netlist if both inverting and non-inverting signals are to be sent from the source to the sink.

Remarks

Applicant's amendment does nothing to overcome the rejections under 35 USC 112, second paragraph or the substantive art rejections under 35 USC 102 and 35 USC 103.

Claims 1-20 recites a generic method that conditionally sends inverting and non-inverting signals from a source to a sink. However, Applicants have failed to establish apriori the existence of any signals in the "moving an inverting buffer" method. Applicants must first recite method steps and elements in the independent claims that setup the required embodied netlist for the conditional "if" step.

Sano and Dupenloup individually and or in combination disclose and/or suggest Applicants' claimed invention as cited, supra. Further, the rejection of claims 1-20 is maintained.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday at 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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